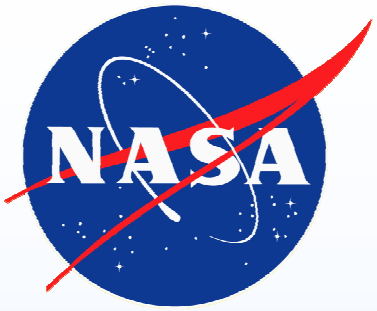

Radiation Characterization of a 0.11 μm Commercial CMOS Process

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Presented by Christian Poivey at the 2006 Single Event Effects Symposium (SEESYM), April 10,2006 to April 12, 2006 in Long Beach, CA.

Outline

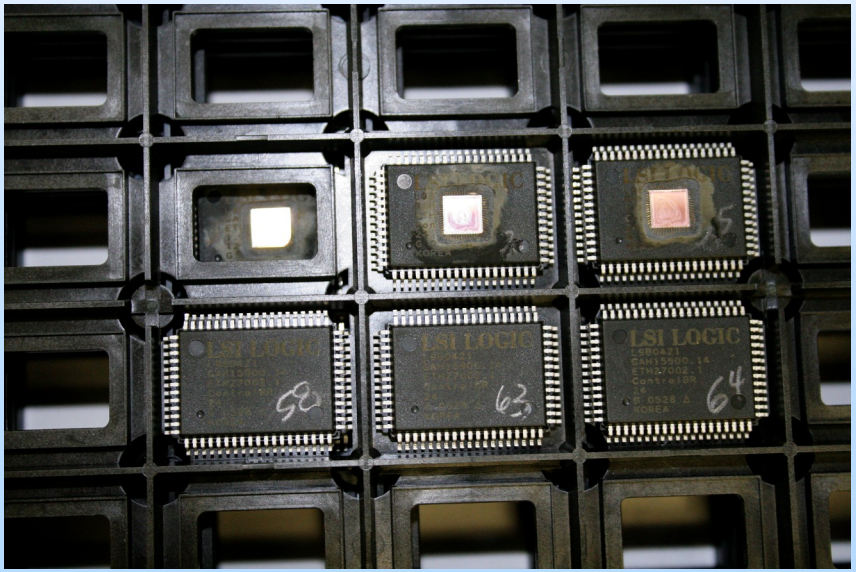
- Background
- Test vehicles
- Test conditions
- Test results
- Conclusion

Background

- NASA-NEPP commercial foundries, scaled CMOS
- 2004:
  - Evaluation of LSI Logic 0.18 μm standard process
    - 0.18 μm drawn bulk process with Shallow Trench Isolation (STI)
    - 1.8V core voltage, up to 3.3V I/O voltage
    - Up to 16 million gates on a chip
  - Evaluation of 0.18 μm modified process with a buried layer
- 2005:
  - Evaluation of LSI Logic 0.11 μm standard process
    - 0.11 μm drawn bulk process with STI
    - 1.2V core voltage, up to 3,3V I/O voltage
    - Up to 70 million logic gates on a chip
    - High density embedded SRAM
  - and two different versions of a modified 0.11 μm process with buried layer

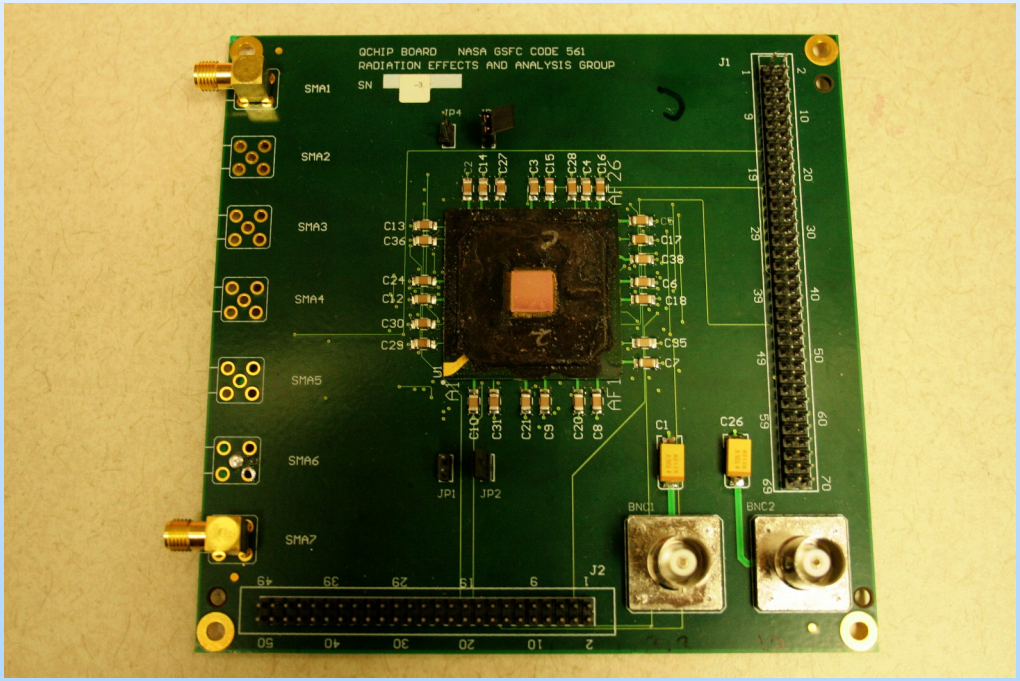
Test Vehicles

- **SRAMs**
  - **4 Mbit (512K*8) made with standard embedded cells**
    - **RAM249, high speed design, cell area=2.49 μm²**
    - **RAM187, high density design, cell area=1.87 μm²**
    - **I/O voltage = 2.5V**
    - **64 PQFP**



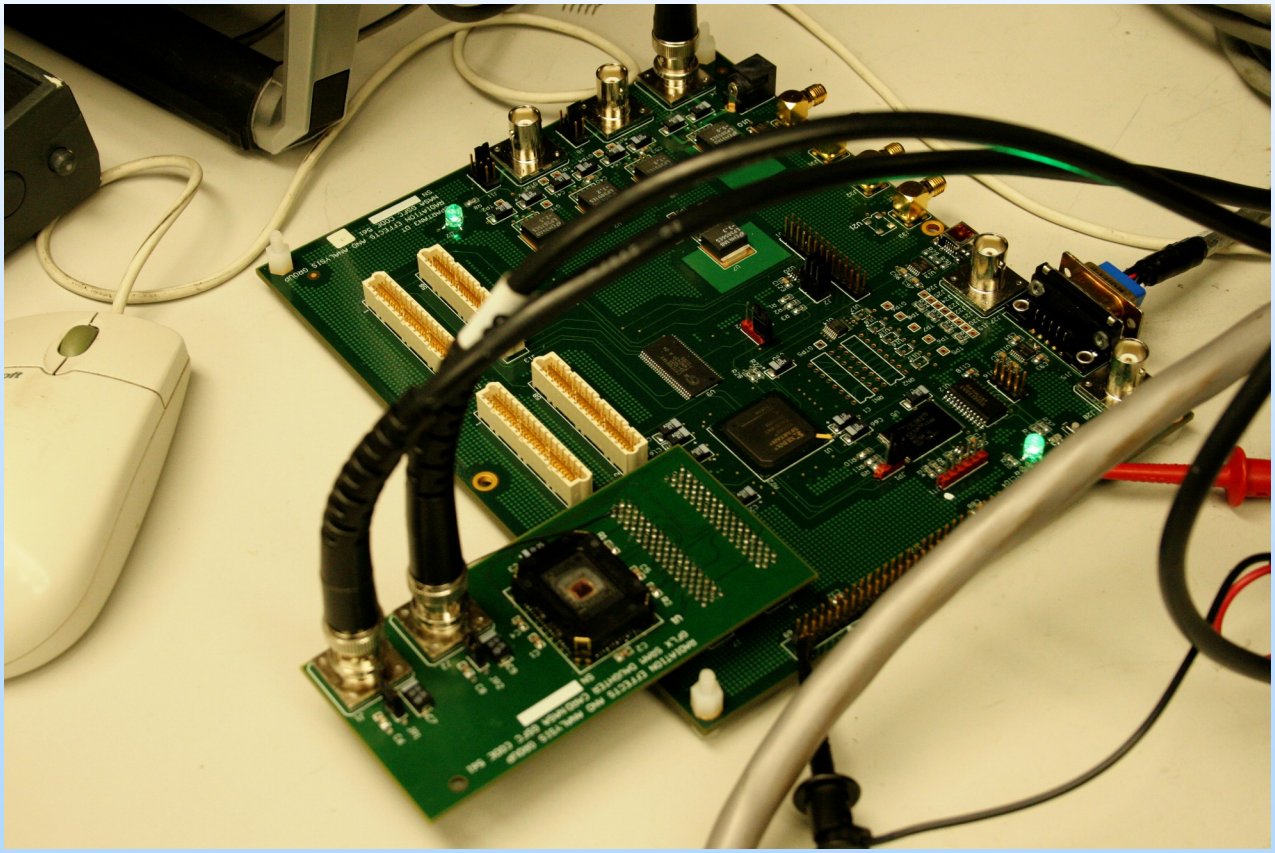
Test Vehicles

- **Logic chip**
  - **Made of 384 64-bit ALUs with registered inputs, outputs, and function control signals. Scan mode capability**
  - **Scan D type flip-flop with set and clear, flip-flop area=55.9 μm^2**
  - **I/O voltage = 3.3V**
  - **492 EPBGA**

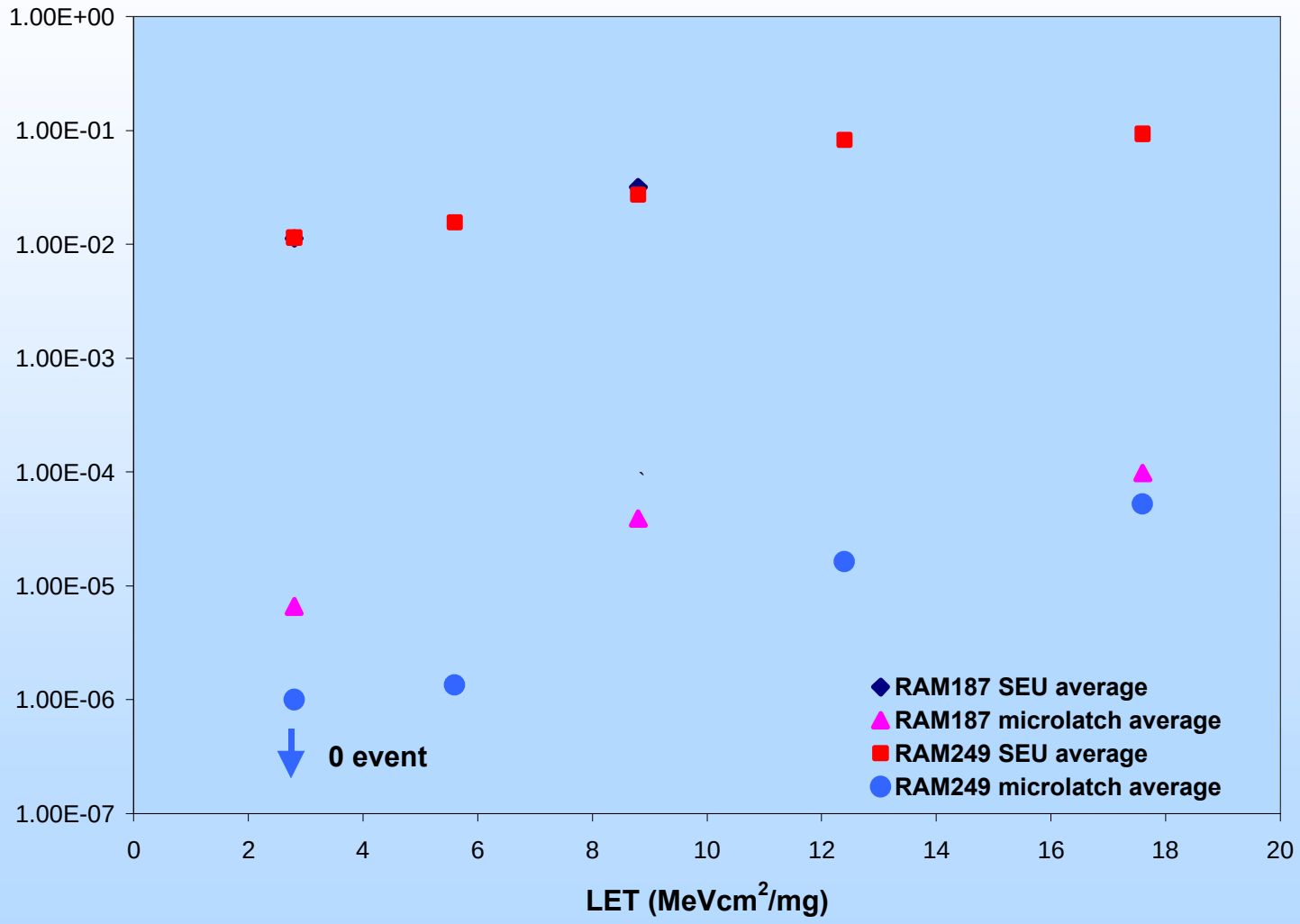


Test conditions

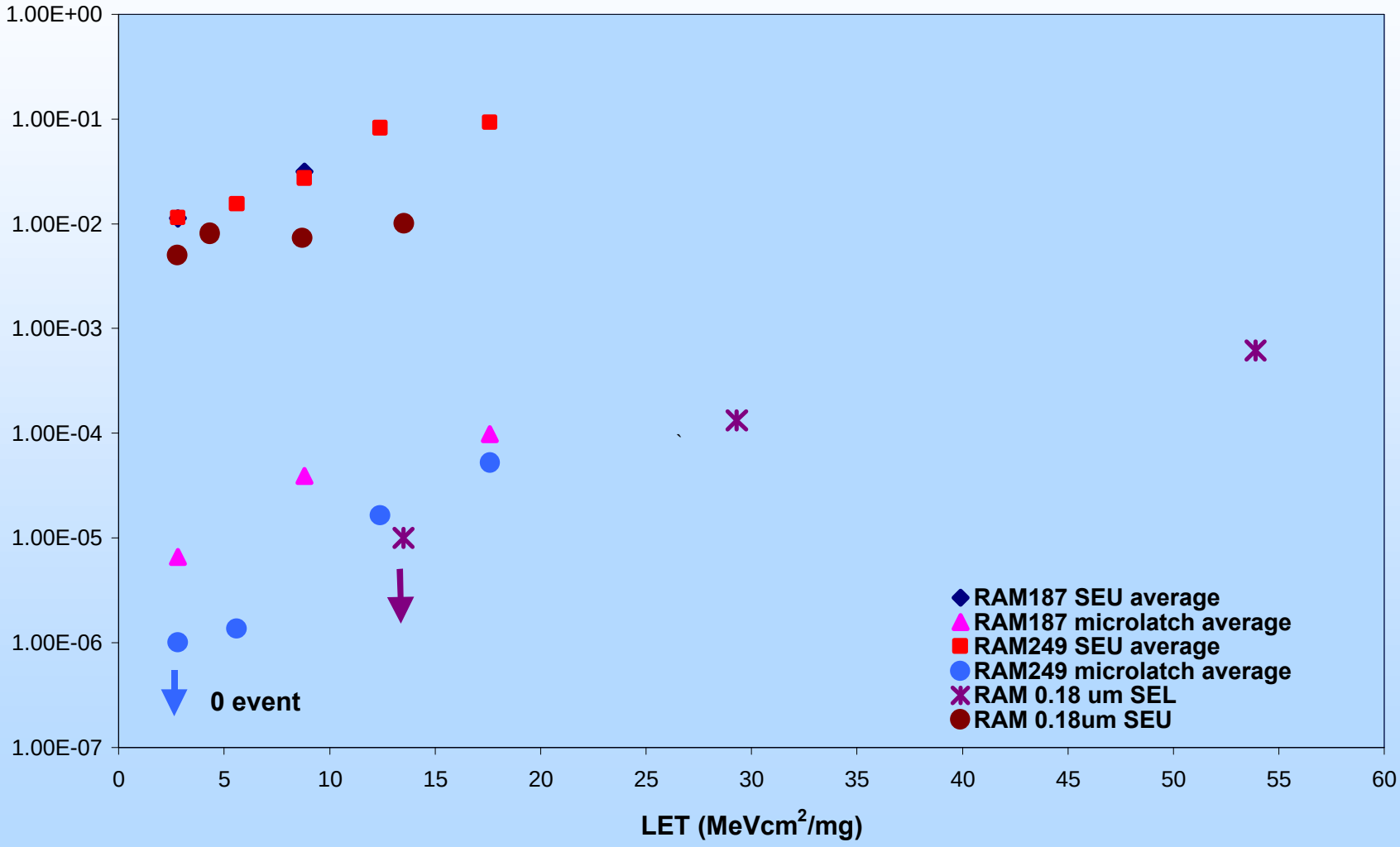
- Used NASA-GSFC low cost digital tester (LCDT)
- SRAM: static and dynamic (10MHz clock cycle)
- Logic chip: test in scan mode (6 shift register chains of 200 flip-flop each) at 2 to 16 MHz clock speed.



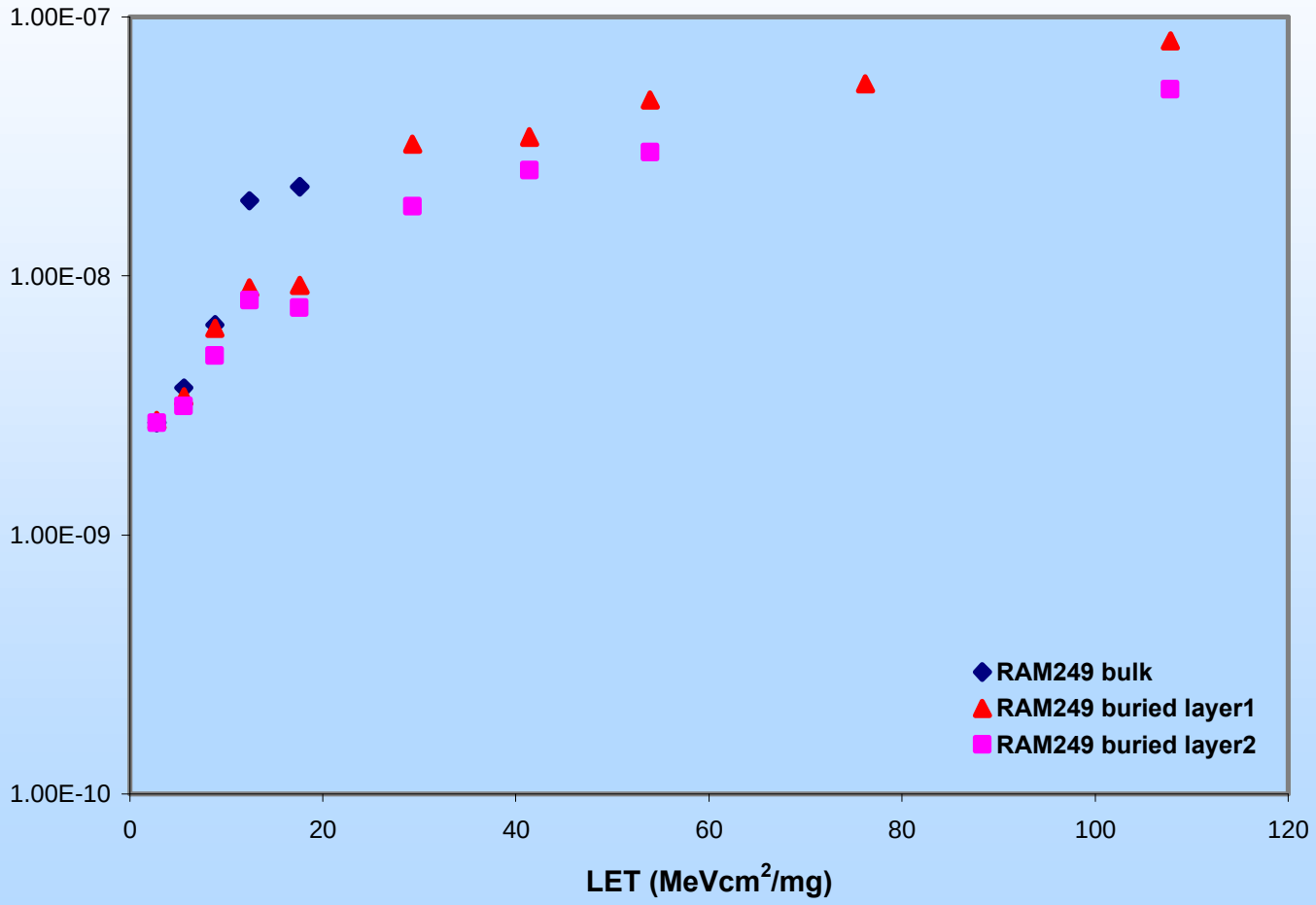
Test results SRAM standard process



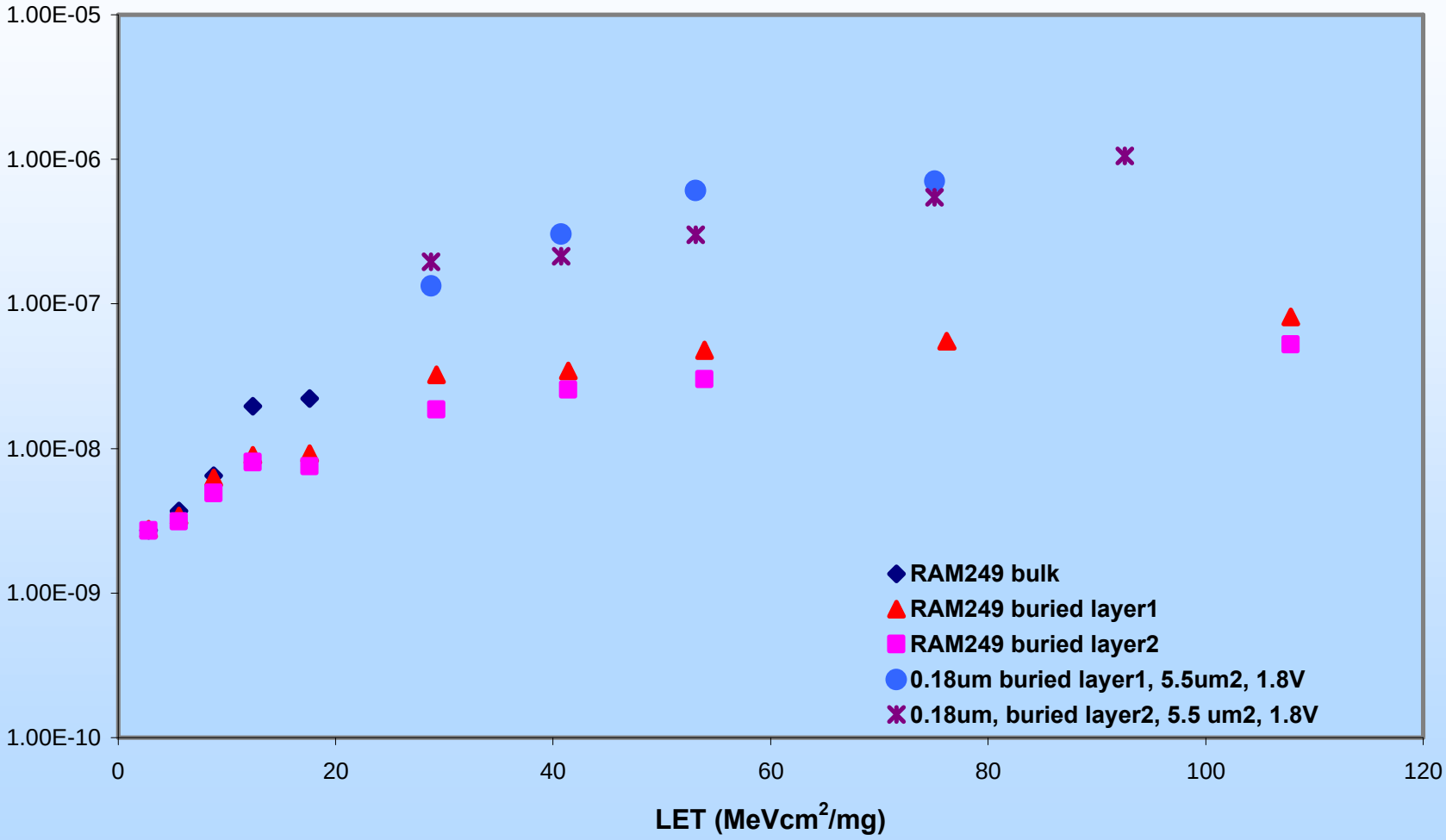
SRAM, SEL, 0.11 μm versus 0.18 μm



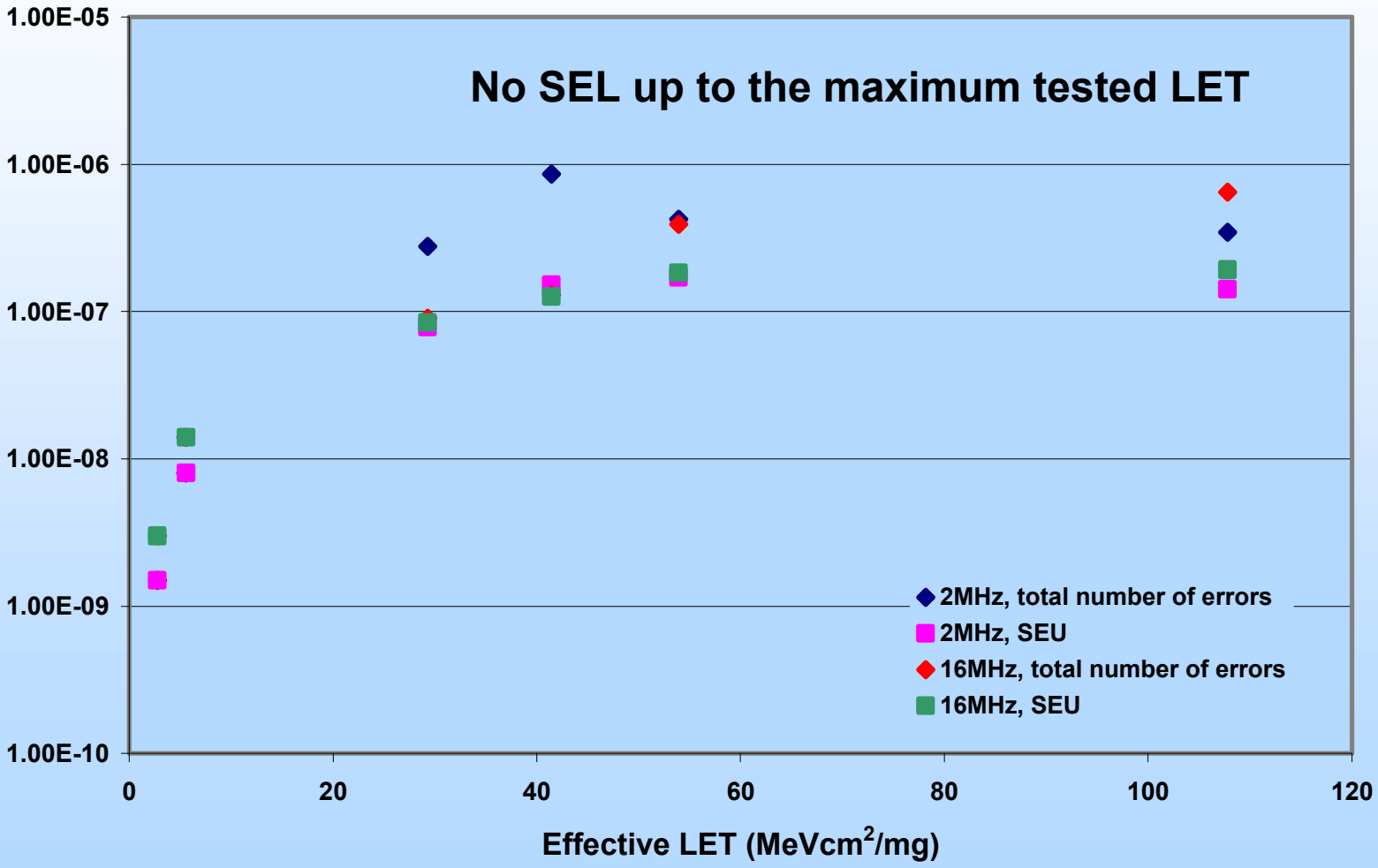
SRAM, RAM249, SEU, all processes



SRAM, SEU, 0.11 μm versus 0.18 μm

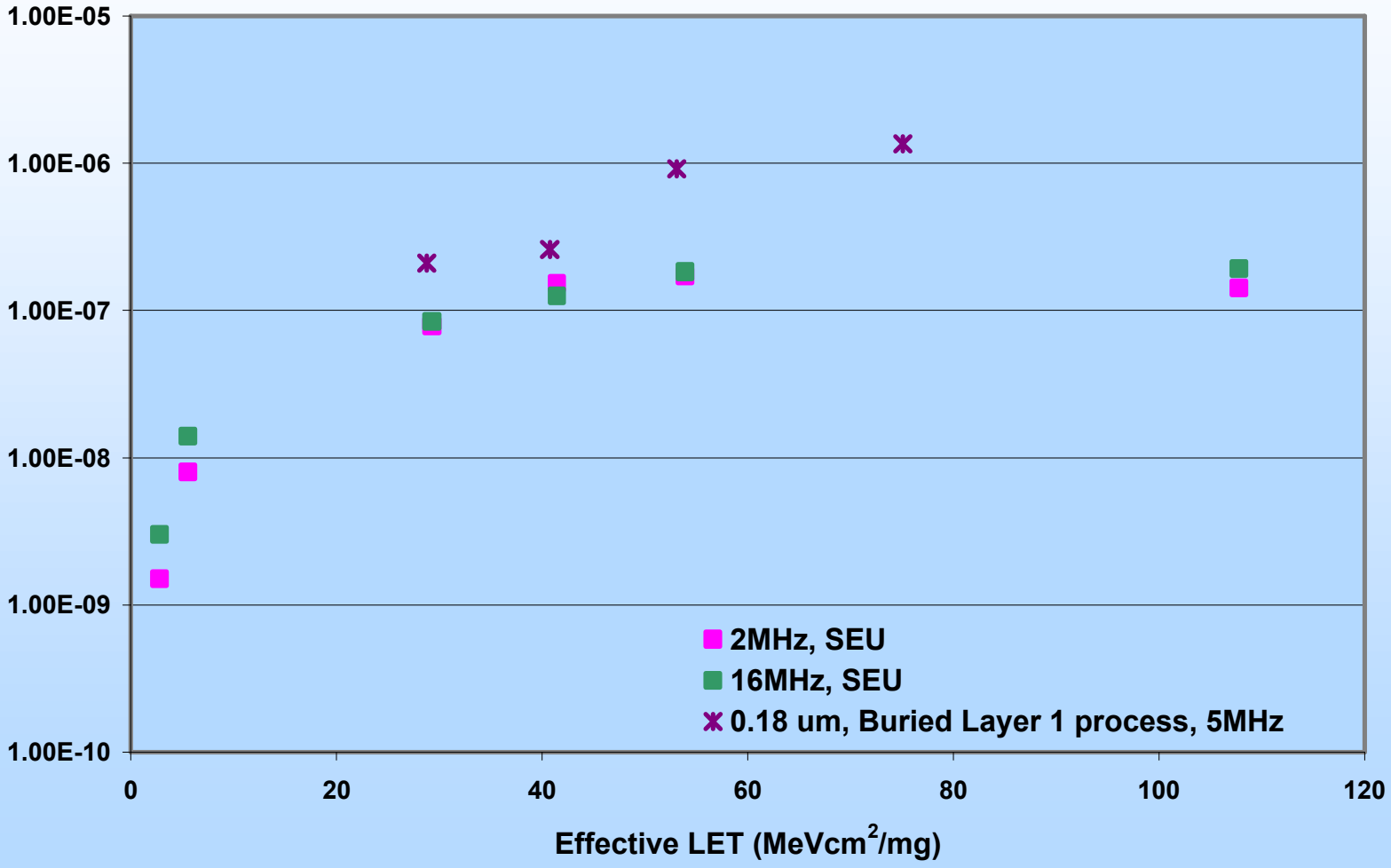


Logic chip, standard process



Logic chip, 0.11 μm versus 0.18 μm

0.18um bulk process is sensitive to SEL down to a LET of 5 MeVcm²/mg



Conclusion

- **0.11 μm process with 1.2V core voltage can still be sensitive to SEL or micro-latchup events**
- **Very low SEU LET threshold**
- **Significant diffusion effect at high LET**
- **Significant transient sensitivity even at low speed**